GT-32090 Single-Chip System Controller

- 16-33 MHz Bus Frequency, No Wait State in Most Cases
- Flexible DRAM Controller Supports Page Mode and EDO
- 128 Mbytes Address Space, 32-Bit Data Width
- Supports ROM/Flash/SRAM and High-Performance I/O Devices
- Supports 8-, 16-, and 32-Bit Devices
- High Performance DMA With Three Independent Channels
- DMA Chaining Via Link Lists of Records
- Data Alignment and Endianess Conversion on the Fly
- Programmable DMA Channel Priorities
- Simple 16-Bit I/O Bus ("80186" Style) For Low Cost Peripherals
- Supports Two PCMCIA Cards Directly
- JTAG, 5V and 3.3V, 160-Pin PQFP

The GT-32090 is a low cost, highly integrated single-chip System Controller for the i960® Jx Processor Family. It provides high system performance, while reducing cost, complexity, device count, and board space. The GT-32090 controls two separate and independent buses, the CPU's 16 to 33 MHz 32-bit wide address/data bus, and a 16-bit I/O bus. The two buses can work concurrently at different frequencies.

The DRAM Controller supports up to 128 Mbytes of standard or EDO DRAM in up to four 32-bit wide banks, with zero wait states to first data or burst data at 16 and 20 MHz. At 25 and 33 MHz, there is one wait state to first data and no wait states to burst data. Various refresh and addressing modes are supported.

The Device Controller supports up to 4 devices directly, and includes various programmable timing and wait state mechanisms that can be setup individually for each device. Typical devices supported include DRAM, ROM, Flash, and SRAM, as well as high-performance master peripherals.

The powerful three-channel DMA Controller has data alignment capabilities and sophisticated chaining support via link lists. The DMA can move data between devices on the CPU bus, or between devices on the CPU bus and devices on the I/O bus. DMA transfers can go through an on-board 16-byte FIFO, or directly if in fly-by mode. Packing and unpacking of 8-bit and 16-bit data from/to the I/O bus occurs concurrently with activity on the CPU bus, increasing overall system bandwidth.

The I/O bus is a simple 80186-like 16-bit bus that interfaces to a large variety of low cost support components like UARTs, SCSI controllers, Ethernet controllers, and other devices. The I/O bus supports 8- or 16-bit peripherals, as well as slave DMA and PCMCIA devices. Three 4-byte FIFOs provide efficient support for the gathering of 8-bit or 16-bit data to/from different peripherals, in the Endianess chosen by the designer.

PROCESSORS SUPPORTED:
i960 Jx Processors

AVAILABILITY:
Samples: September 1995
Production: December 1995

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